This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-6 (Canceled)

7. (Original): A step-up circuit, comprising:

a step-up clock signal generation device that generates a clock signal to be used for voltage step-up;

at least one step-up stage that steps up a power supply voltage based on the clock signal; and

a control device that, after starting an operation, changes a frequency of the clock signal to be supplied to the step-up stage from a value lower than a normal value to the normal value.

8. (Original): A step-up circuit according to claim 7, wherein the control device includes:

a plurality of frequency-divider circuits that frequency-divide the clock signal generated by the step-up clock signal generation device, and respectively output a plurality of divided clock signals having different frequency division ratios,

a selector circuit that selects, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

a counter that counts the clock signal selected by the selector circuit to thereby generate the control signal; and

wherein the step-up stage steps up the power supply voltage based on the clock signal selected by the selector circuit.

9. (Original): A step-up circuit according to claim 7, wherein the control device includes:

a plurality of frequency-divider circuits that frequency-divide a clock signal applied, and respectively output a plurality of divided clock signals having different frequency division ratios,

a selector circuit that selects, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

a counter that counts the clock signal selected by the selector circuit to thereby generate the control signal; and

wherein the step-up clock signal generation circuit generates, based on the clock signal selected by the selector circuit, a clock signal to be used for voltage step-up.

10. (Original): A step-up circuit according to claim 7, wherein the control device includes:

a plurality of frequency-divider circuits that frequency-divide a clock signal applied, and respectively output a plurality of frequency-divided clock signals having different frequency division ratios,

a counter that counts pulse signals applied, and

a selector circuit that selects, based on an output value of the counter, one of the clock signal and the plurality of frequency-divided clock signals; and

wherein the step-up clock signal generation circuit generates, based on the clock signal selected by the selector circuit, a clock signal to be used for voltage step-up.

Claims 11-16 (Canceled)

17. (Original): A step-up circuit, comprising:

means for generating a step-up clock signal to be used for voltage step-up;

means for successively stepping up a power supply voltage based on the clock signal; and

a means for controlling that, after starting an operation, changes a frequency of the clock signal to be supplied to the means for successively stepping up from a value lower than a normal value to the normal value.

18. (Original): A step-up circuit according to claim 17, wherein the means for controlling includes:

means for frequency-dividing the clock signal generated by the means for generating a step-up clock signal, and respectively output a plurality of divided clock signals having different frequency division ratios,

means for selecting, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

means for counting the clock signal selected by the means for selecting to thereby generate the control signal; and

wherein the means for successively stepping up steps up the power supply voltage based on the clock signal selected by the means for selecting.

19. (Original): A step-up circuit according to claim 17, wherein the means for controlling includes:

means for frequency-dividing the clock signal a clock signal applied, and respectively output a plurality of divided clock signals having different frequency division ratios,

means for selecting, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

means for counting the clock signal selected by the means for selecting to thereby generate the control signal; and

wherein the means for successively stepping up generates, based on the clock signal selected by the means for selecting, a clock signal to be used for voltage step-up.

20. (Original): A step-up circuit according to claim 17, wherein the means for controlling includes:

means for frequency-dividing the clock signal a clock signal applied, and respectively output a plurality of frequency-divided clock signals having different frequency division ratios,

means for counting pulse signals applied, and

means for selecting, based on an output value of the means for counting, one of the clock signal and the plurality of frequency-divided clock signals; and

wherein the means for successively stepping up generates, based on the clock signal selected by the means for selecting, a clock signal to be used for voltage step-up.

Claims 21-26 (Canceled)

27. (Original): A method of operating a step-up circuit, comprising:

generating a step-up clock signal to be used for voltage step-up;

successively stepping up a power supply voltage based on the clock signal; and

changing, after starting an operation, a frequency of the clock signal to be supplied to the successively stepping up from a value lower than a normal value to the normal value.

28. (Original): A method of operating a step-up circuit according to claim 27, wherein the changing includes:

frequency-dividing the clock signal generated by the generating a step-up clock signal, and respectively outputing a plurality of divided clock signals having different frequency division ratios,

selecting, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

counting the clock signal selected by the selecting to generate the control signal; and

wherein the successively stepping up steps up the power supply voltage based on the clock signal selected.

29. (Original): A method of operating a step-up circuit according to claim 27, wherein the changing includes:

frequency-dividing the clock signal applied, and respectively outputting a plurality of divided clock signals having different frequency division ratios,

selecting, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

counting the clock signal selected to thereby generate the control signal; and

wherein the successively stepping up generates, based on the clock signal selected, a clock signal to be used for voltage step-up.

30. (Original): A method of operating a step-up circuit according to claim 27, wherein the changing includes:

frequency-dividing the clock signal applied, and respectively outputting a plurality of frequency-divided clock signals having different frequency division ratios,

counting pulse signals applied, and

selecting, based on an output value of the counting, one of the clock signal and the plurality of frequency-divided clock signals; and

wherein the successively stepping up generates, based on the clock signal selected, a clock signal to be used for voltage step-up.